CLAIMS

What is claimed is:

1. A method for processing a substrate, comprising:
providing a substrate of a first material having a bare surface;
applying a layer of a second material to the bare surface;
bonding the layer of the second material to the bare surface; and
removing the first material and the second material from the substrate at substantially equal rates.

2. The method of claim 1, wherein removing the first material and the second material from the substrate at substantially equal rates comprises planarizing the substrate from the bare surface.

3. The method of claim 2, wherein planarizing the substrate from the bare surface comprises substantially reducing an initial thickness of the substrate.

4. The method of claim 1, wherein removing the first material and the second material from the substrate at substantially equal rates comprises substantially reducing an initial thickness of the substrate.

5. The method of claim 1, wherein providing a substrate of a first material having a bare surface comprises providing a semiconductor substrate.

6. The method of claim 5, wherein providing a semiconductor substrate comprises providing a wafer of silicon, gallium arsenide, germanium or indium phosphide.

7. The method of claim 5, wherein the bare surface comprises a backside of the semiconductor substrate.

8. The method of claim 1, further comprising oxidizing the bare surface prior to applying the layer of the second material.

9. The method of claim 1, wherein the second material comprises a polymeric material.

10. The method of claim 1, wherein the second material includes at least one of the polymer groups comprising epoxies, acrylics, silicones, urethanes, siloxanes and Parylenes™.

11. The method of claim 1, wherein the second material is a flowable material and is applied to the bare surface by one of screen-coating, stencil-coating, and spin-coating.

12. The method of claim 1, wherein the second material is at least a semisolid element and applying comprises laminating the at least a semisolid element to the bare surface.

13. The method of claim 12, wherein the at least a semisolid element comprises one of a tape and film.

14. The method of claim 12, wherein the at least a semisolid element comprises a layer of the second material placed on a backing layer, and applying comprises applying the layer of the second material to the bare surface and removing the backing layer.

15. The method of claim 14, further comprising applying a release layer to the backing layer before placing the second material thereon, and wherein removing the backing layer comprises releasing the layer of the second material from the backing layer using the release layer.

16. The method of claim 1, wherein the second material is one of a thermoset polymer and a radiation cross-linkable polymer, and wherein the second material is applied to the bare surface in a flowable state and cured to a hardened state.

17. The method of claim 1, wherein the second material comprises an epoxy, and the epoxy is partially cured to a tacky state prior to application to the bare surface and further cured to bond to the bare surface and harden.

18. The method of claim 1, further comprising hardening the second material on the bare surface.

19. The method of claim 18, wherein hardening the second material comprises curing the second material.

20. The method of claim 1, further comprising filling irregularities in a surface topography of the bare surface by applying the layer of second material thereto.

21. The method of claim 1, wherein applying the layer of the second material to the bare surface comprises substantially covering the bare surface with the second material.

22. The method of claim 1, wherein removing the first material and the second material from the substrate at substantially equal rates comprises at least one of wet etching, dry etching, grinding, abrasive planarization, and chemical-mechanical planarization.

23. The method of claim 1, further comprising removing first material from the substrate prior to applying the second material to the bare surface.

24. The method of claim 23, wherein removing first material from the substrate prior to applying the second material to the bare surface is effected by a process including mechanical abrasion of the substrate.

25. The method of claim 24, wherein removing the first material and the second material from the substrate at substantially equal rates comprises etching.

26. The method of claim 23, wherein removing the first material and the second material from the substrate at substantially equal rates comprises planarizing the substrate from the bare surface.

27. The method of claim 26, wherein removing the first material and the second material from the substrate at substantially equal rates comprises etching.

28. The method of claim 23, wherein removing the first material and the second material from the substrate at substantially equal rates comprises etching.

29. An in-process semiconductor wafer comprising an active surface having integrated circuitry fabricated thereon and a backside surface having a layer of a material bonded thereto and filling irregularities in a topography thereof.

30. The in-process semiconductor wafer of claim 29, wherein an exposed surface of the layer of the material is substantially planar.

31. The in-process semiconductor wafer of claim 29, wherein the layer of the material substantially covers the backside surface.

32. The in-process semiconductor wafer of claim 29, wherein the material exhibits a material removal rate substantially equal to a material removal rate exhibited by the semiconductor wafer for a selected material removal process.

33. The in-process semiconductor wafer of claim 29, wherein the material comprises at least one of the polymer groups comprising epoxies, acrylics, silicones, urethanes, siloxanes and Parylenes™.